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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,132	04/02/2004	Todd P. Lukanc	H1777	1494

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EXAMINER	
GARBOWSKI, LEIGH M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

14-A

Office Action Summary	Application No.	Applicant(s)	
	10/817,132	LUKANC ET AL.	
	Examiner	Art Unit	
	Leigh Marie Garbowski	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20-22* is/are allowed.

6)☒ Claim(s) *1-5,9-11 and 14* is/are rejected.

7)☒ Claim(s) *6-9,12,13,15-19 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892) 2 sheets
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/01/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The abstract of the disclosure is objected to because "can including" [line 1] is confusing. Correction is required. See MPEP § 608.01(b).

The disclosure is objected to because of the following informalities: in accordance with figure 2, "215" [page 6, line 17, 24, 27] should be --225-- and "225" [page 6, line 18] should be --215--.

Appropriate correction is required.

Claim Objections

Claims 9, 12, 15, 18, 22 are objected to because of the following informalities: as per claim 9, the antecedent basis for "indicating layouts" [line 2] is not clear since step (c) provides for "identifying portions" [claim 1]; as per claim 12, there is no antecedent basis for "step (a)" [line 1]; as per claim 15, there is no antecedent basis for "step (c)" [line 1]; as per claim 18, there is no antecedent basis for the features described in "being indicative of layout patterns that fail at least one ORC demonstrating good and poor manufacturability [lines 3-5]; and as per claim 22, there is no antecedent basis for "at least one pre-existing design rule from the current technology" [line 2]. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 9-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Galan et al. [U.S. Patent #6,899,981 B1].

As per claim 1, a method of producing an IC device layout corresponding to an IC device design, said method comprising: (a) generating an initial layout corresponding to the IC device design, said initial layout complying with a predetermined set of design rules [column 4, line 47]; (b) simulating how structures within the initial layout will pattern on a wafer [column 4, lines 47-59]; (c) identifying portions of the simulated layout which demonstrate poor manufacturability [column 4, lines 50-59; column 6, lines 53-56; column 8, lines 39-41; column 9, lines 8-12]; and (d) creating at least one design rule to disallow at least one portion of the layout identified in step (c) [column 5, lines 1-3, 15-18; column 6, lines 1-3, 25-30, 50-53, 59-64; column 7, lines 27-31; column 9, lines 8-21]. As per claim 2, said method further comprising: (e) producing a layout complying with the design rules created at step (d) [column 5, lines 30-43; column 6, lines 56-59; column 9, lines 25-30]; and (f) simulating how structures within the layout produced at step (e) will pattern on a wafer [column 4, lines 47-59; column 6, lines 59-64]. As per claim 3, said method further comprising: repeating steps (c)-(f) until no portions of the simulated layout demonstrate poor manufacturability [loop in figure 3]. As per claim 5, said method further comprising: performing at least one OPC on the layout before performing step (b) [column 3, lines 34-37]. As per claim 9, said method further comprising: providing a graphical representation [column 5, lines 20-21; column 9, lines 22-25]. As per claim 10, wherein the initial layout is embodied in a layout data file [column 4, line 47].

Claims 1-5, 10-11, 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Misaka et al. [U.S. Patent #6,691,297 B1].

As per claim 1, a method of producing an IC device layout corresponding to an IC device design, said method comprising: (a) generating an initial layout corresponding to the IC device design, said initial layout complying with a predetermined set of design rules [column 4, lines 24-26; column 12, lines 66-67]; (b) simulating how structures within the initial layout will pattern on a wafer [column 13, lines 7-21]; (c) identifying portions of the simulated layout which demonstrate poor manufacturability [column 13, line 58-column 4, line 14, 43]; and (d) creating at least one design rule to disallow at least one portion of the layout identified in step (c) [column 15, lines 28-33; column 16, lines 20-21, 27-28]. As per claim 2, said method further comprising: (e) producing a layout complying with the design rules created at step (d) [column 13, lines 1-6]; and (f) simulating how structures within the layout produced at step (e) will pattern on a wafer [column 13, lines 7-21]. As per claim 3, said method further comprising: repeating steps (c)-(f) until no portions of the simulated layout demonstrate poor manufacturability [column 16, lines 21-22, 28-29]. As per claim 4, said method further comprising: modifying at least one design rule of the predetermined set of design rules to disallow a portion of the layout identified in step (c) [column 15, lines 30-33; column 16,lines 20-21, 27-29]. As per claim 5, said method further comprising: performing at least one OPC on the layout before performing step (b) [column 4, lines 26-32]. As per claim 10, wherein the initial layout is embodied in a layout data file [column 12, lines 66-67]. As per claim 11, a method of producing design rules, said method comprising: generating a plurality of parametrically varying layout patterns [column 16, lines 36-44]; simulating how each layout pattern will pattern on a wafer [column 13, lines 7-21]; classifying edges of structures within the simulated layout patterns based on manufacturability [column 13, lines 15-16, 58-column 4, line 14; column 16, lines 54-57]; and creating design rules to disallow layout patterns demonstrating poor manufacturability [column 15, lines 28-33; column 16, lines 20-21, 27-28, 54-58]. As per claim 14, said method further comprising: performing at least one OPC on the geometric layouts prior to the simulating step [column 4, lines 26-32].

Allowable Subject Matter

Claims 6-8, 12-13, 15-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 20-22 are allowed.

The following is an examiner's statement of reasons for allowance: the prior art of record does not disclose, teach, or suggest a method of generating a set of design rules for a next generation technology, said method comprising: (a) providing a design library of layout patterns corresponding to a current technology; (b) scaling one or more layout patterns of the design library to the next generation technology; (c) generating simulation images of the scaled layout patterns from step (b); (d) performing ORCs on the simulation images from step (c); (e) identifying layout patterns which fail one or more ORCs; and (f) creating one or more design rules to disallow the layout patterns identified in step (e).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leigh Marie Garbowski whose telephone number is 571-272-1893 and e-mail is Leigh.Garbowski@uspto.gov. The examiner can normally be reached on days.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LEIGH M. GARBOWSKI
PRIMARY EXAMINER